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☐ **5. Promising Complex ASIC Design Verification Method**

Assaf, M.H.; Das, S.R.; Hernias, W.; Jone, W.B.;
[Instrumentation and Measurement Technology Conference Proceedings, 2007](#)
1-3 May 2007 Page(s):1 - 6
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☐ **6. A reusable pseudo-random verification environment for
designs: The SpaceWire interface case study**

Saponara, Sergio; Vitullo, Francesco; Petri, Esa; Fanucci, Luca;
[Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications](#)
[IDAACS 2009. IEEE International Workshop on](#)
21-23 Sept. 2009 Page(s):102 - 106
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